BlueVD4 Board

User Manual
BLUEVD4-BRD-UM
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RivieraWaves
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Revision history

Version	Date	Revision description	Author
1.00	2010-04-01	Initial Release	JPL
1.01	2010-06-24	Typos correction in switch explanation table	JPL

Changes between a version and the previous one is reflected by the addition of **change bars**, like for the line below:

…This line has been modified from previous version…

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1 Overview

1.1 Document overview

This document describes the connections and set up for the BlueVD4 board kit, consisting of a BlueVD4 board, a transformer, an application daughter board, and an optional RF daughter board for BlueJay TC1.

1.2 System pictures

The following picture shows the BlueVD4 board in standalone mode.

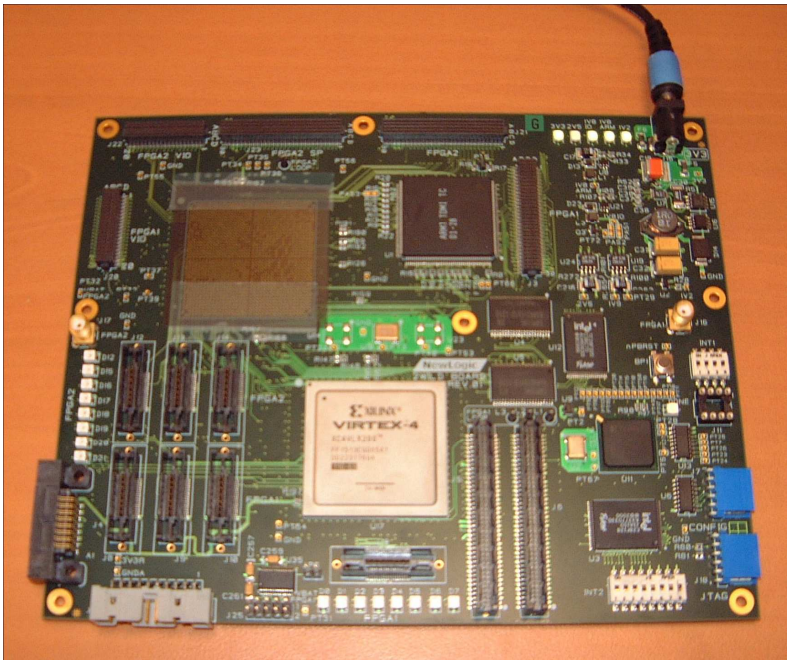

Figure 1.1 – BlueVD4 board

2 BlueVD4 board quick start

On the following board diagram, the useful connectors and switches are highlighted in order to quickly find them on the actual board. The necessary connections are detailed below.

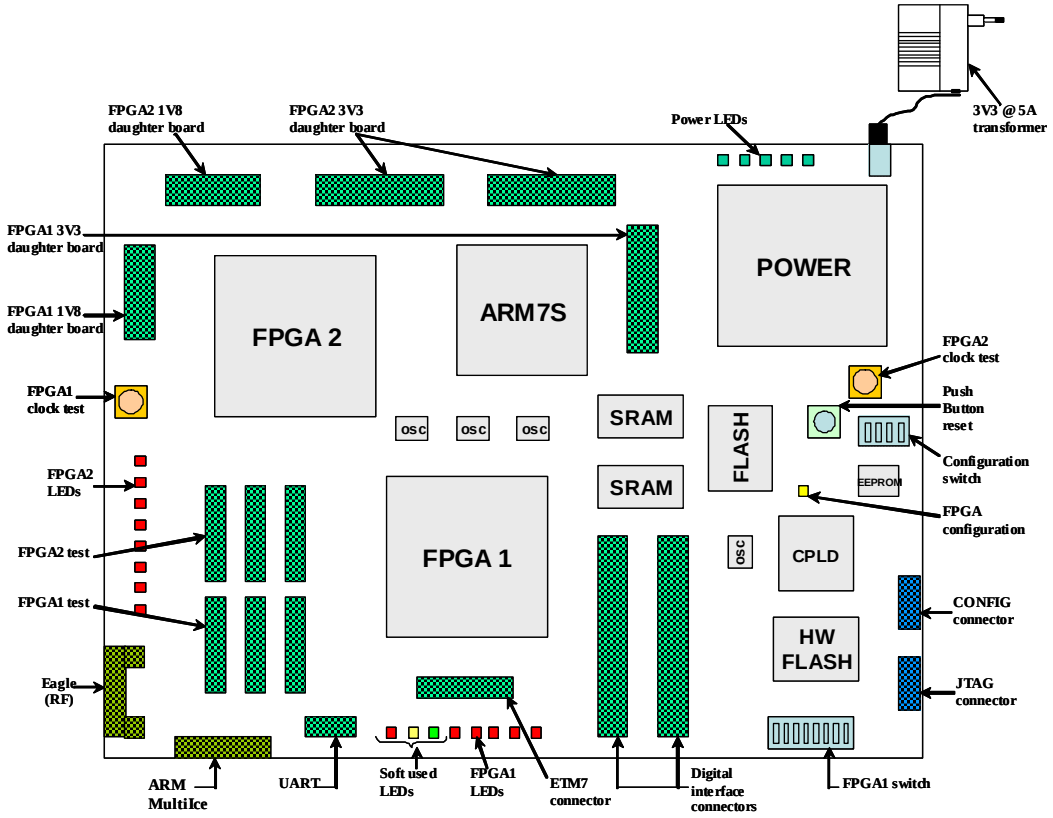

Figure 2.1 – BlueVD4 overview

2.1 Power up

The power up of the BlueVD4 board is very simple. Power the board with the correct transformer: 3V3 @ 5A to supply the board.

- ✓ Transformer part reference: SB-035A0F-11, 3V3 @ 5A from Stontronics
- ✓ Jack connector + inside, - outside

IMPORTANT: Never connect a transformer with higher voltage than 3V3 to supply the BlueVD4 board, it will be severely damaged.

Once the board is powered, the FPGA is loaded with the binary stored in the HW Flash. At the end of loading, the orange LED “FPGA configuration” becomes on and indicates that the FPGA is correctly configured and ready to start.

If the LED “FPGA configuration” is not ON at the power up of the board, please refer to chapter 9.2.

2.2 Programming HW Flash

The necessary tools to program the HW Flash on the board are:

- ✓ BLUE POD: Small RivieraWaves HW box used to connect a PC to the board.
- ✓ FlashProg: RivieraWaves Software program running on the PC, minimum version 4.6.

The following list details how to connect the Blue POD to the BlueVD4 board:

- ✓ **Check in the BIOS of your computer that the parallel port is set in EPP mode before launching Windows™.**
- ✓ Connect the BLUE POD to the serial link connector called CONFIG connector (J7) on Figure 2.1.
- ✓ Connect the other side of the BLUE POD to the parallel port of the PC. **Please check that no other application is using the parallel port at the same time.**
- ✓ Place switch 4 of INT1 to ON. INT1 switch is called configuration switch on Figure 2.1.

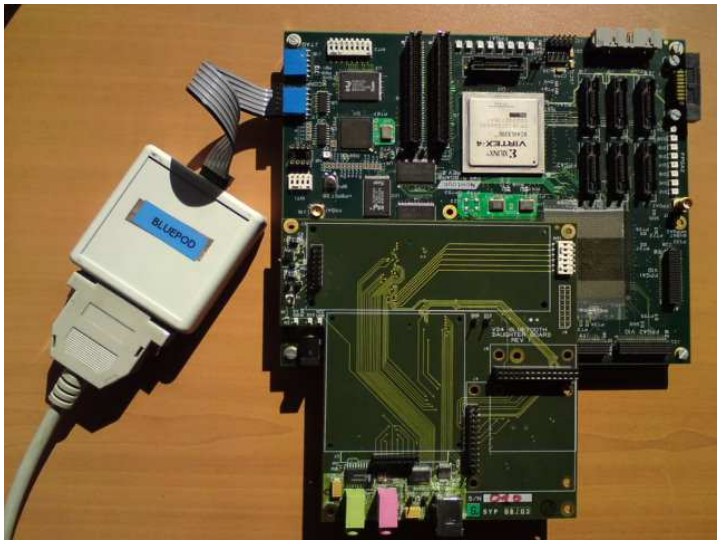

Figure 2.2 – BlueVD4 board with BLUE POD

The final step to program the HW Flash is to launch the FlashProg software:

- ✓ Power up the board with the correct supply.
- ✓ Launch FlashProg on the connected PC. **Minimum version of FlashProg must be 4.6**.
- ✓ Select the FPGA1 tick box (please refer to 1 on Figure 2.3).
- ✓ Select the correct Platform: WiLDSYSFPGA, see 2 on Figure 2.3.
- ✓ Going through "…", select the corresponding HW binary (.bit file*) for FPGA1. Refer to 3 on Figure 2.3. FPGA2 field is useless for the BlueVD4 platform, as FPGA2 is not mounted.
- ✓ Click on the program button.
- ✓ At the end of the programming, the orange LED ("FPGA configuration") must be on, indicating that the FPGA is programmed with the new file stored inside the HW Flash.

***** Don't forget the necessary option in Xilinx ISE to generate the .bit file : Startup options → FPGA Start Up Clock → CCLK

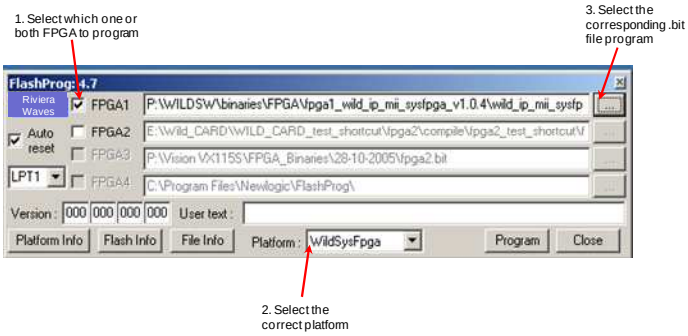

Figure 2.3 – FlashProg interface

3 ARM7S chip JTAG

The BlueVD4 features an ARM7TDMI processor, directly mounted on the board (external ARM7TDMI). The user can also synthesize its own ARM7S processor and can integrate it directly in the FPGA (internal ARM7S).

Whatever the type of processor used, being internal or external, the processor JTAG is accessible through a "MultiIce" connector, see Figure 2.1. This JTAG chain provides a serial line to the processor, and eases the real time debugging.

3.1 Case of external ARM7S

To use the external ARM7S JTAG chip, connect the ARMS_CHIP_TDO FPGA input to the ARMS_TDO FPGA output.

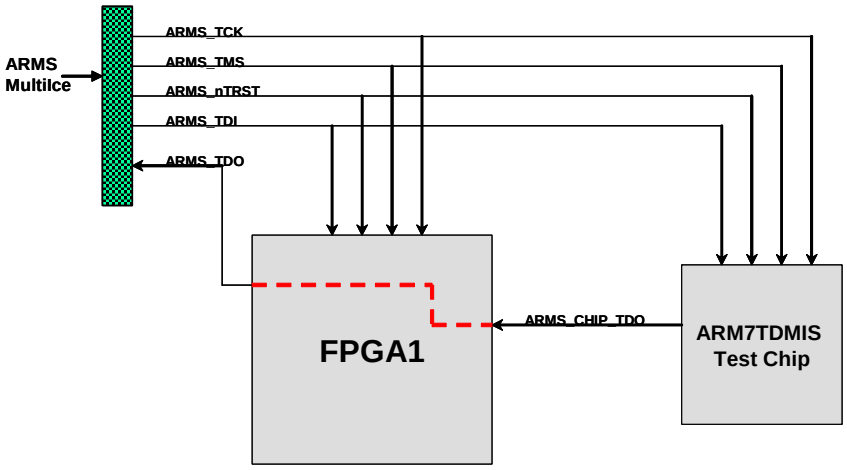

Figure 3.1 – External ARM7S JTAG

3.2 Case of internal ARM7S

In case of internal ARM7S use only, just connect the JTAG lines to the ARM7S block, leave unconnected the ARMS_CHIP_TDO from the external ARM7S.

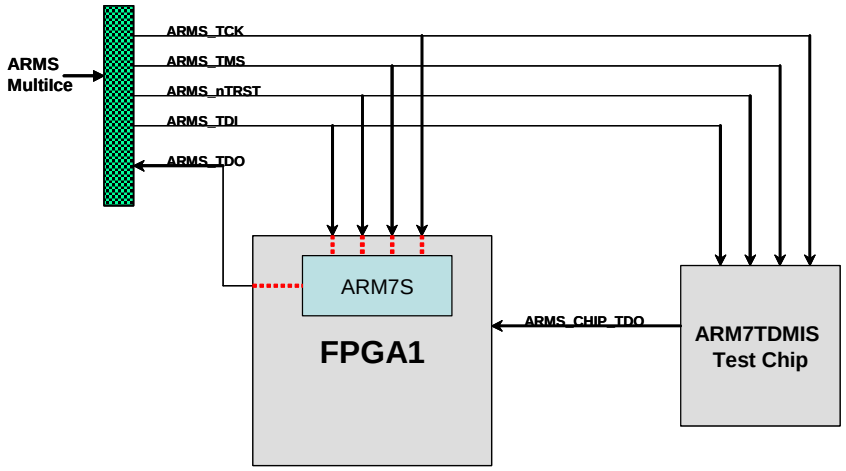

Figure 3.2 – Internal ARM7S JTAG

3.3 Case of internal and external ARM7S

In that case, connect the JTAG data of the both ARM7S in serial mode as shown below.

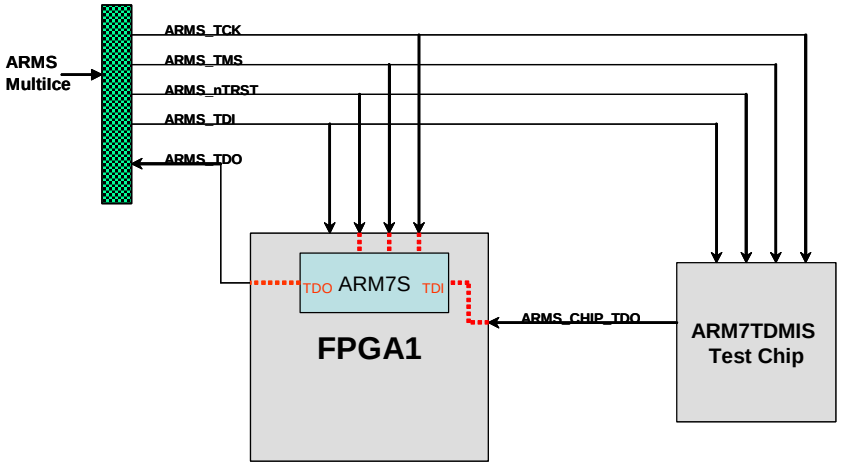

Figure 3.3 – Internal and external ARM7S

4 Xilinx JTAG chain

4.1 FPGA JTAG chain

The Xilinx JTAG chain can be used for programming the binary and provides also read back capabilities, if used with the correct ISE tool from Xilinx.

To see the FPGA JTAG chain, connect your parallel PC cable and Xilinx box to the JTAG connector (J18) on board, see Figure 2.1.

There is a FGPA JTAG chain only for the FPGA1 or both for FPGA1 and FPGA2. By default, the FPGA JTAG chain of the board is configured only for FPGA1: R80 mounted and R81 not mounted. To connect FPGA2 to the XILINX JTAG chain, just reverse the two resistors: R80 not mounted and R81 mounted. R81 and R80 are zero Ohm resistors.

Important: FPGA2 is not mounted on the BlueVD4 prototyping board.

With IMPACT software from Xilinx, it is possible to load the FPGAs directly with their programs, without using the CPLD and the HW Flash. Note that the .bit file must be generated with the necessary option in Xilinx ISE: Startup options → FPGA Start Up Clock → JTAG.

The main disadvantage of this kind of FPGA loading is that programs are lost once the power is removed, and it is necessary to reload the program inside the FPGA with IMPACT software at each power up. Note that the JTAG programming is very slow compared to programming through the CPLD.

4.2 CPLD JTAG Chain

The CPLD JTAG chain is separate from the FPGA JTAG chain due to different supply voltages (3V3 for CPLD and 2V5 for FPGA). Access to the CPLD is done via IMPACT software from XILINX. The same connector is used for both the HW Flash loading and CPLD configuration, i.e CONFIG connector (J7), see Figure 2.1. To switch to the CPLD chain instead of HW Flash loading chain, put switch 4 of INT1 OFF (INT1 switch is called configuration switch on Figure 2.1).

The CPLD is already loaded with the RivieraWaves program and has the following features:

- ✓ Automatically loads program(s) from the HW Flash to the FPGA(s) at power up.
- ✓ Transfers the FPGA programs from the PC into the HW Flash component.
- ✓ Handles system reset of the board. For more information about system reset, see chapter 5.
- ✓ PCMCIA configuration start, when digital interface is used as PCMCIA (CVS and CCD signals).

5 System reset

The CPLD handles the system reset of the BlueVD4 board.

The different reset sources are going to the CPLD, and the CPLD transmits them to the main components on board.

Reset sources:

- ✓ Voltage supervisor reset.
- ✓ End of FPGA configuration signal.
- ✓ Push Button Reset.
- ✓ PCMCIA reset coming from Digital interface (if Digital interface is used as PCMCIA).
- ✓ Reset coming from the RF (Eagle) interface.

Component resets handled by CPLD:

- ✓ FPGA1
- ✓ FPGA2
- ✓ HW_Flash
- ✓ Radio board

For the radio board, the choice is offered between a reset coming directly from CPLD (load R103 and remove R104) or a resent passing through FPGA (load R104 and remove R103).

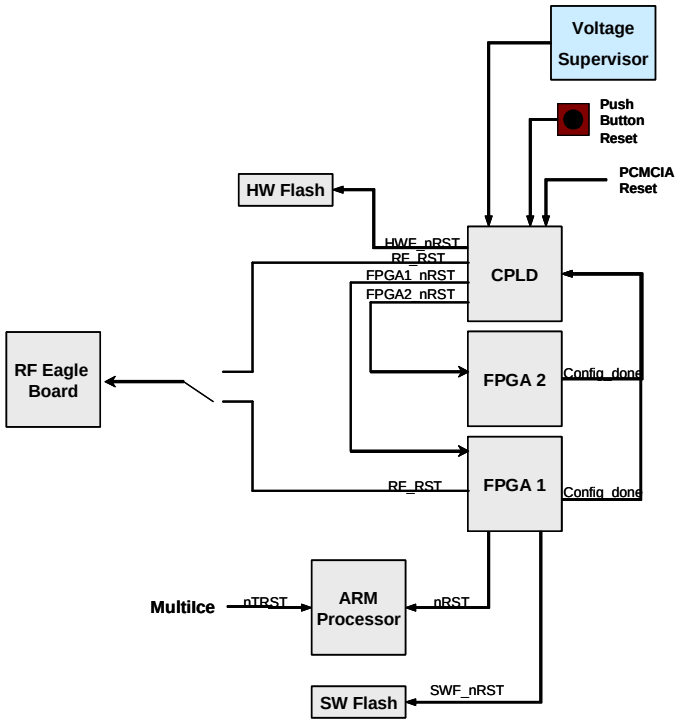

Figure 5.1 – System reset

6 Switches and LEDs

6.1 Switches

An eight lines switch is connected to FPGA1. An ON position means that the line is connected to 3V3 through a 10K resistor. An OFF position means that the line is connected to ground through a 10K resistor.

A second four line switch is present on board and the lines are distributed as following:

- ✓ First two lines (1 & 2) connected to CPLD
- ✓ Third line (3) connected to FPGA2
- ✓ Fourth line (4) allows the choice between: ON: HW Flash loading with BLUE POD, OFF: CPLD JTAG chain.

An ON position on the second switch means directly connected to ground, and an OFF position means connected to 3V3 through 10K resistor.

6.2 LEDs

Each FPGA has eight external LED connections.

FPGA1 has a first set of three different color LEDs (red, yellow, green) followed by five others red LEDs.

FPGA2 has eight red LEDs.

7 Daughter boards

For future daughter boards, there are five available connectors on the BlueVD4 board.

- ✓ Two are connected to FPGA1.
- ✓ Three are connected to FPGA2.

Both small connectors (64 pins) are each connected to an entire bank of each FPGA. That is to say that all the signals of the bank and consequently of the connector can have the same voltage standard which is on board configurable.

Four holes are available on the BlueVD4 board to attach the daughter board.

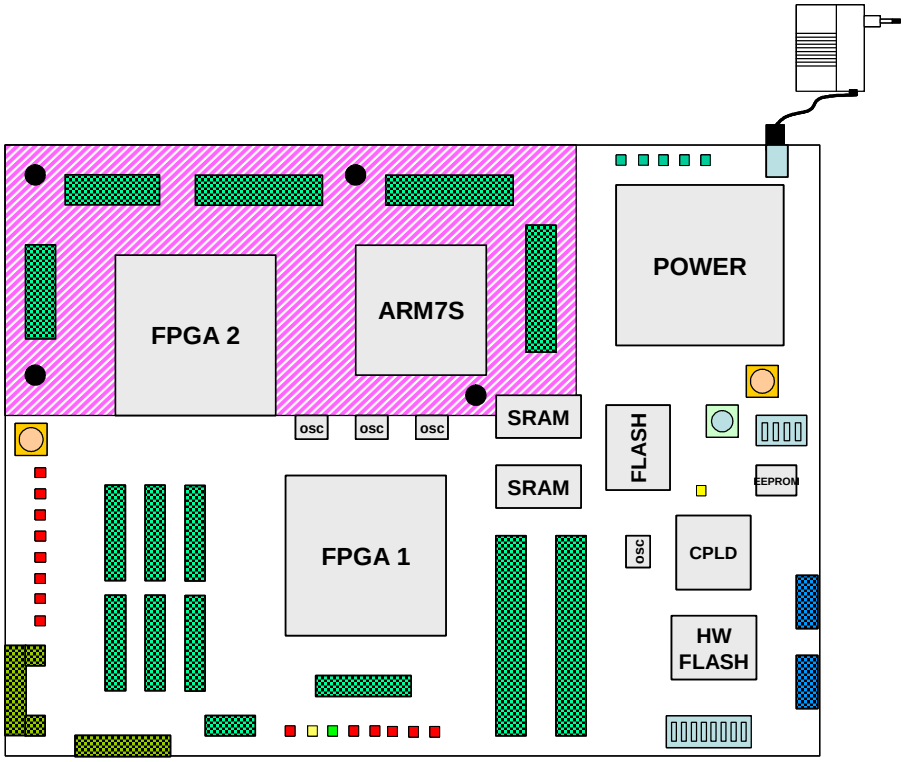

Figure 7.1 – Future daughter board

7.1 BlueVD4 application daughter board

This section describes the daughter board that enables the BlueVD4 development board, to add complete Bluetooth functionality. The code name of this board is VD4BTDB. Figure 7.2 depicts the envisioned system:

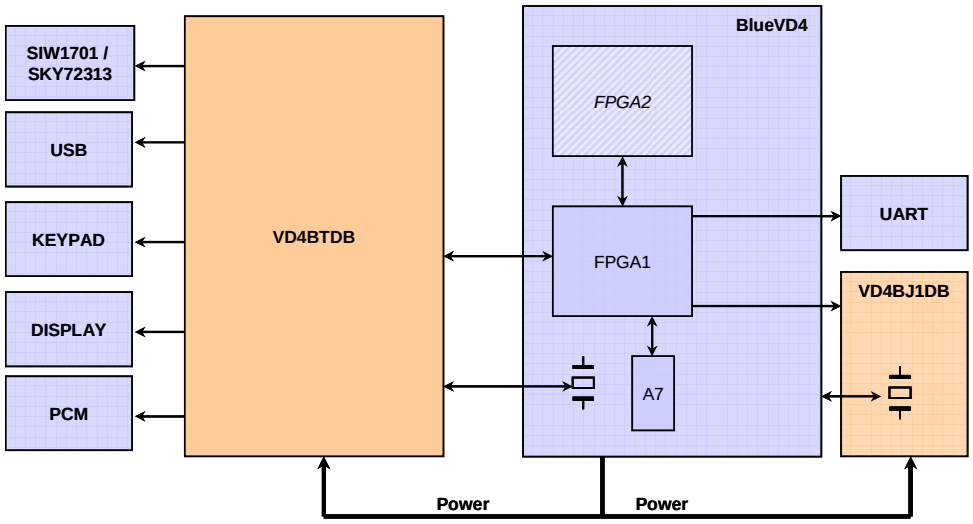

Figure 7.2 – BlueVD4 Bluetooth System

7.1.1 Features description

7.1.1.1 HCI Support

7.1.1.1.1 FTDI

An external FIFO-to-USB chip will be used to convey the Bluetooth HCI. FT245BM Chip [2] from FTDI plus USB Series B connector female are used.

Integrating the USB chip directly on the VD4BTDB, has the advantage to avoid adding another daughter board. In this case, just an external crystal and passive components are needed.

7.1.1.1.2 Integrated USB Device

To support the configuration in which a standard USB Device controller would be instantiated within BlueVD4, an USB Series B connector female and Philips Transceiver: PDIUSBP11ADB are needed in the VD4BTDB. USB standard version is 1.1.

In case of the FT245BM being integrated in the VD4BTDB, the interface to the USB connector should be routed either from the FTDI port or from the Philips transceiver (configurable, see Table 7.1).

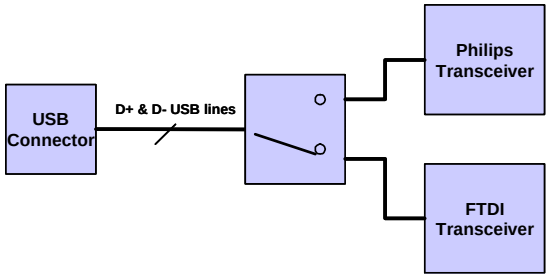

Figure 7.3 – USB configuration

7.1.1.2 Supported radio modules

7.1.1.2.1 Fallback BT1.2

7.1.1.2.1.1 SiW1701

Interface with the Silicon Wave radio board:

- 13 digital control lines
- 2x12 Male connector (kind HE14)
- A 32.768KHz oscillator is to be mounted on BlueVD4. The goal is to replace the low power clock from Silicon Wave board not always present (depends on the board version). Low power clock selection between internal / external source is to be performed inside BlueVD4 as per Silicon Wave board version.

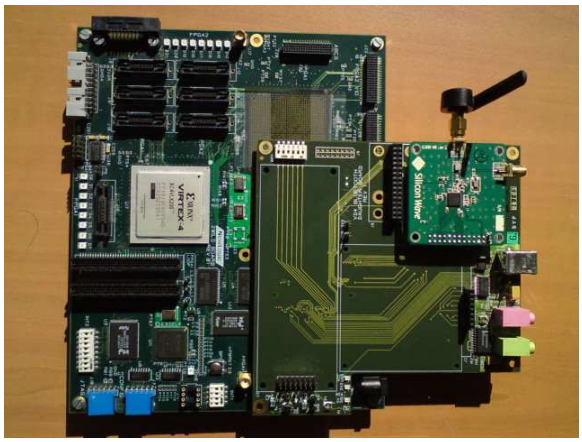

Figure 7.4 – Siw RF module plugged on VD4BTDB

7.1.1.2.1.2 Semtech XE1413

Interface with Semtech XE1413

- 11 digital control lines
- 2x15 Female connector (kind HE14)
- The low power oscillator of the Semtech radio board is used. The local BlueVD4 oscillator can be used as an alternative.

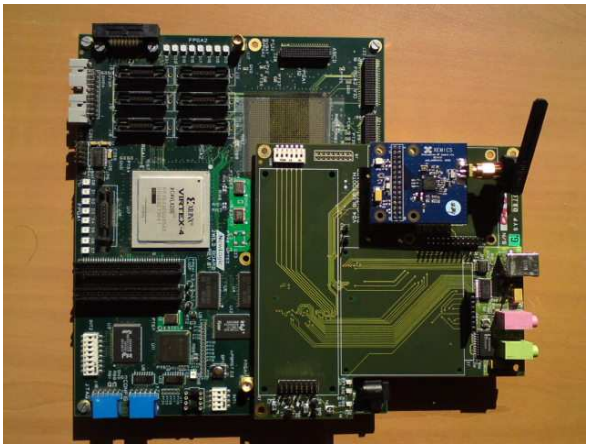

Figure 7.5 – Xemics/Semtech RF module plugged on VD4BTDB

7.1.1.2.1.3 RivieraWaves Bluejay Bluetooth radio

To be connected to BlueVD4 through a dedicated daughter board. This requirement falls outside the scope of VD4BTDB, but is captured here for reference purposes. The interface with the Bluejay TC1 radio board is as follows:

- 14 digital control lines
- Male/connector (MOLC_120_02_S_Q_LC, 80 pin)
- The 32.768KHz clock is taken from the oscillator to be mounted on BlueVD4.

7.1.1.3 MMI devices (optional)

Keypad and LCD could be either:

- Mounted via a ribbon cable as side components
- Screwed over the VD4BTDB

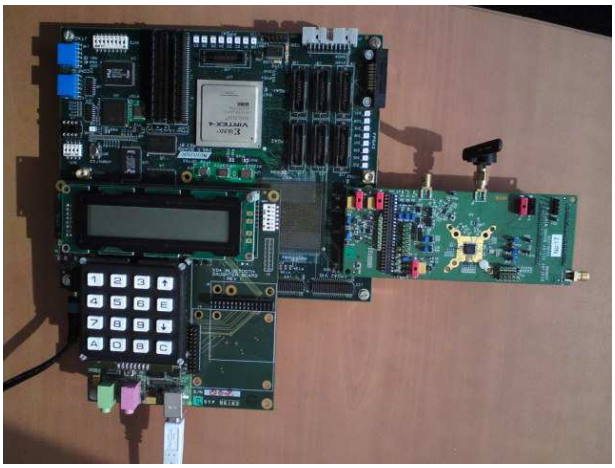

Figure 7.6 – Keypad and display mounted for full embedded applications

7.1.1.4 Keypad (optional)

Interface with Keypad is a simple 8x1 connector. The 8x1 connector is defined to drive:

- 4 vertical lines
- 4 horizontal lines

Keypad features:

- Matrixed
- 16 buttons

7.1.1.5 Display (optional)

As for the keypad, there is a display connector on the VD4BTDB to connect a display.

The display is already a mini board with a complete digital interface:

- 11 lines (8 data bits plus 3 control lines Select, read, write).

Should the option of mounting the LCD above VD4BTDB be retained, the potentiometer used to tune it shall not be covered, allowing easy access to the rotating wiper.

7.1.1.6 PCM

A PCM interface is available on the BCARDDB with a PCM codec and Jack connectors. This interface allows a user to connect a headset.

PCM Codec: MC145483 from Motorola

Audio jacks: two 3.5mm 3 PTS audio jacks (green for speaker, pink for microphone, PC color convention)

To ensure structural solidity, the audio jacks need to be mounted through the PCB, not just surface soldered.

7.1.1.7 Configuration capabilities

The configuration switch INT1 allows:

- Selecting the radio interface,
- Selecting the way of connecting to the host system, UART or FTDI,
- Selecting how is routed the PCM output from the FPGA,
- Selecting the source of the main reset.

The Table 7.1 describes the configurations available.

Switch	Value	Action
1	On	Select UART to support HCI
	Off	Select FTDI to support HCI, this is the default value
2	On	Select PCM routed to audio codec
	Off	Select PCM routed to dedicated connector, this is the default value
3, 4, 5	On-On-On	RADIO_CONF: Select the connected RF chip. On-On-On: SiW // Off-On-On: XE1314 // On-Off-On: BJ TC1
	Off-On-On	
	On-Off-On	
6	On	Reset coming from on board reset button
	Off	Reset coming from BlueJay RF reset button, this is the default value when BlueJay RF module is used

Table 7.1 – Configuration switches

Important: Switch to On means logical value '0', whereas switch to Off means logical value '1'.

7.1.1.8 Power supplies

The 3V3 voltage present on the BlueVD4 is passed to the VD4BTDB through the daughter board connectors. One pin per connector is dedicated to 3V3 voltage.

The 5V needed by the FT245BM USB chip is coming directly from the USB interface (i.e. from the PC).

The 5V needed by the display, is done with a Linear step-up regulator: LT1930ES5 from the 3V3 analog present on board.

Power sources available in BlueVD4 are listed in section 7.1.2.2.

7.1.2 Digital signals

The following table lists all the digital signals coming from BlueVD4. It also explains how these signals are mapped on the connector interface between BlueVD4 and VD4BTDB.

Digital Interface	Number of signal from FPGA	Signal list
USB Philips Transceiver	8	RCV, OE, SUSPEND, VM, VP, VMO, VPO, SPEED
USB FTDI	14	D[7,0], RD#, WR, TXE#, RXF#, PWREN#, RESET#
KEYPAD	8	V[3,0], H[3,0]
DISPLAY	11	DB[7,0], E, RS, RW
SKY72313/XE1413/BTRF	2	SYS_CLK_OUT/BB_CLK, SYNC_FOUND/ENABLE_RM
SPI Bus for fallback 1.2 Radio	4	SPI_SMD, SPI_MSD, SPI_SS_N, SPI_CLK
Control Bus for fallback 1.2 Radio	6	CD_TXEN, RX_TX_DATA, TX_DATA_UNI, BB_32K, HOP_STRB, RM_RESET
PCM_Bus	4	PCM_DOUT, PCM_CLK, PCM_DIN, PCM_FSYNC
Switch	6	2 for radio selection, 4 free.
Diagnostic	8	8 output ports for logic analyzer
TOTAL	71	

Table 7.2 – Digital signal list

7.1.2.1 Digital signal correspondence table

The following table explains the relation between VD4BTDB and BlueVD4 signals, stating the correspondence between signal names in the schematics, connector pins and FPGA pins. The connector J3 is used to plug VD4BTDB on top of the BlueVD4 motherboard. The corresponding bus in the BlueVD4 schematic is FPGA1_DGHT.

VD4BTDB Digital Interface	VD4BTDB Signal name	VD4BTDB Connector Pin	BlueVD4 connector Pin	FPGA1_DGHT(i)	FPGA1 Connector Pin
PDIU_USB_BUS : USB Philips Transceiver	PDIU_RCV	J1-A12	J3-A12	11	U17-L/D1
	PDIU_OE	J1-A13	J3-A13	12	U17-L/E4
	PDIU_SUSPEND	J1-B14	J3-B14	38	U17-L/K7
	PDIU_VM	J1-A14	J3-A14	13	U17-L/E3
	PDIU_VP	J1-A15	J3-A15	14	U17-L/F2
	PDIU_VMO	J1-A16	J3-A16	15	U17-L/F1
	PDIU_VPO	J1-A17	J3-A17	16	U17-L/F6
	PDIU_SPEED	J1-A18	J3-A18	17	U17-L/F5
FTDI_USB_BUS : USB FTDI Transceiver	FTDI_D7	J1-C15	J3-C15	64	U17-P/N4
	FTDI_D6	J1-C16	J3-C16	65	U17-P/N3
	FTDI_D5	J1-D17	J3-D17	91	U17-P/T9
	FTDI_D4	J1-C17	J3-C17	66	U17-P/N2
	FTDI_D3	J1-D18	J3-D18	92	U17-P/T8
	FTDI_D2	J1-D19	J3-D19	93	U17-P/T6
	FTDI_D1	J1-D20	J3-D20	94	U17-P/T5
	FTDI_D0	J1-D21	J3-D21	95	U17-P/T4
	FTDI_nRXF	J1-D22	J3-D22	96	U17-P/T3
	FTDI_nTXE	J1-C22	J3-C22	71	U17-P/P6
	FTDI_nRD	J1-D23	J3-D23	97	U17-P/T1
	FTDI_WR	J1-C23	J3-C23	72	U17-P/P5
	FTDI_nRESET	J1-C24	J3-C24	73	U17-P/P4
	FTDI_nPWREN	J1-C25	J3-C25	74	U17-P/P2
KEYPAD_BUS : Bus for external Keypad	KEY_V3	J1-A6	J3-A6	5	U17-L/B3
	KEY_V2	J1-A7	J3-A7	6	U17-L/C4
	KEY_V1	J1-B8	J3-B8	32	U17-L/I7
	KEY_V0	J1-A8	J3-A8	7	U17-L/C3
	KEY_H3	J1-A9	J3-A9	8	U17-L/C2
	KEY_H2	J1-B10	J3-B10	34	U17-L/I5
	KEY_H1	J1-A10	J3-A10	9	U17-L/D4
	KEY_H0	J1-A11	J3-A11	10	U17-L/D2
LCD_BUS : Bus for external Display	LCD_DB7	J1-C1	J3-C1	50	U17-L/M11
	LCD_DB6	J1-D2	J3-D2	76	U17-L/R16
	LCD_DB5	J1-C2	J3-C2	51	U17-L/M10
	LCD_DB4	J1-D3	J3-D3	77	U17-L/R14
	LCD_DB3	J1-C3	J3-C3	52	U17-L/M8
	LCD_DB2	J1-D4	J3-D4	78	U17-L/R12
	LCD_DB1	J1-C4	J3-C4	53	U17-L/M7
	LCD_DB0	J1-D5	J3-D5	79	U17-L/R11
	LCD_E	J1-C5	J3-C5	54	U17-L/M6
	LCD_RW	J1-D6	J3-D6	80	U17-L/R9
	LCD_RS	J1-D7	J3-D7	81	U17-L/R8
RADIO_BT1.2	BB_CLK(1)	J1-B5	J3-B5	29	U17-P/H4
	ENABLE_RM(2)	J1-B6	J3-B6	30	U17-P/H3
RF_BT1.2_SPI_BUS	SPI_SS_N	J1-B1	J3-B1	25	U17-L/G2
	SPI_CLK	J1-B2	J3-B2	26	U17-L/G1

	SPI_MSD	J1-B3	J3-B3	27	U17-L/H7
	SPI_SMD	J1-B4	J3-B4	28	U17-L/H5
RF_BT1.2_CTRL_BUS	RM_RESET	J1-C11	J3-C11	60	U17-L/N10
	HOP_STRB	J1-C12	J3-C12	61	U17-L/N8
	TX_DATA_UNI	J1-D13	J3-D13	87	U17-L/T15
	CD_TXEN	J1-C13	J3-C13	62	U17-L/N7
	RX_TX_DATA	J1-D14	J3-D14	88	U17-L/T14
	BB_32K	J1-D15	J3-D15	89	U17-L/T13
PCM_BUS : Digital PCM interface	PCM_CLK	J1-A19	J3-A19	18	U17-L/F4
	PCM_FSYNC	J1-B20	J3-B20	44	U17-L/L8
	PCM_DIN	J1-A20	J3-A20	19	U17-L/F3
	PCM_DOUT	J1-B21	J3-B21	45	U17-L/L6
SWITCH6_1 : Switches for control	SWITCH1	J1-C7	J3-C7	56	U17-P/M3
	SWITCH2	J1-D8	J3-D8	82	U17-P/R6
	SWITCH3	J1-C8	J3-C8	57	U17-P/M2
	SWITCH4	J1-D9	J3-D9	83	U17-P/R4
	SWITCH5	J1-C9	J3-C9	58	U17-P/M1
	SWITCH6	J1-D10	J3-D10	84	U17-P/R3
DIAG7_0 : Switches for control	DIAG0	J1-A21	J3-A21	20	U17-P/Y13
	DIAG1	J1-B22	J3-B22	46	U17-P/L5
	DIAG2	J1-A22	J3-A22	21	U17-P/Y11
	DIAG3	J1-B23	J3-B23	47	U17-P/L4
	DIAG4	J1-A23	J3-A23	22	U17-P/Y9
	DIAG5	J1-B24	J3-B24	48	U17-P/L3
	DIAG6	J1-A24	J3-A24	23	U17-P/AA11
	DIAG7	J1-B25	J3-B25	49	U17-P/L1
TOTAL	71				

Table 7.3 – Digital pin correspondence between BlueVD4 and VD4BTDB

Notes:

(1) This signal carries the clock from the RF device to the baseband (it is an input to BlueVD4's FPGA1). Note that this clock may or may not be actually used to clock the entire system: this decision is made inside BlueVD4's FPGA1. The signal names are:

   a. BB_CLK (SiW)

   b. CNX_SYS_CLK_OUT (Semtech)

(2) This signal carries different information depending on the destination RF device. This signal is an output of BlueVD4's FPGA1, where the selection of the actual signal source is carried out:

   a. ENABLE_RM (SiW) : RF Power down indication from baseband

   b. SYNC_DET (Semtech): Baseband signal telling RF device that packet synchronization has been achieved.

7.1.2.2 Power correspondence table

Table 7.4 shows the power supply signals available in BlueVD4's J3 connector:

VD4BTDB Digital Interface	BlueVD4 Signal name	BlueVD4 connector Pin
Power	Vcc_3.3V	J3-B27
	Vcc_3.3V	J3-D27
Ground	GND	J3-A1
	GND	J3-A2
	GND	J3-A3
	GND	J3-B26
	GND	J3-A26
	GND	J3-A27
	GND	J3-D26
	GND	J3-C26
	GND	J3-C27
	GND	J3-C28
	GND	J3-C29
	GND	J3-C30
TOTAL	13	

Table 7.4 – Digital power correspondence between BlueVD4 and VD4BTDB

7.1.3 Part list

The following table summarizes the components used in the VD4BTDB:

Part Number	RivieraWaves Stock	Description
LT1930ES5	Y	Step-up regulator for LCD
FT245BM	BeTech	FTDI UART 2 USB I/F Chip
MC145483DW	Y	Audio codec
ROLC_130_02_S_Q_LC	Y	Male connector 120 pin
ANTELEC BAR 15x2	BeTech	Semtech board connector
HE14 12x2	BeTech	SiW board connector
FCN_724P016_AU/W	BeTech	LCD Connector
HE14 8x1	BeTech	KP Connector
TOBY STX_3150_5N_577C	Y	Audio jack 3.5mm (Microphone)
TOBY STX_3150_5N_701C	Y	Audio jack 3.5mm (Speaker)
PDIUSBP11ADB	Y	Philips USB 1.1 PHY transceiver
MOLEX_CON_USB_TYPE_B	BeTech	USB-TYPE-B connector
FCN_724P016_AU/W	BeTech	Logic Analyzer connector
IKN0604000	BeTech	Switches

Table 7.5 – VD4BTDB Part list

7.2 BlueVD4 BlueJay TC1 daughter board (optional)

7.2.1 Overview

This section describes the Daughter Board that enables

- The characterization of the Bluejay TC1 device
- The BLUEVD4 development board adds Bluetooth RF link functionality by using Blue jay TC1.

The code name of this board is VD4BJ1DB. The two different roles played by this board are outlined below.

The Figure 7.7 shows such a daughter board connected to the BlueVD4 board, on the right side of the picture.

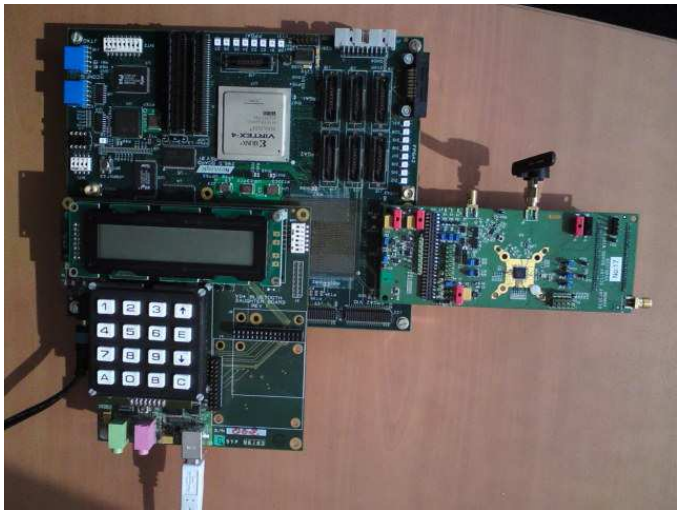

Figure 7.7 – BlueJay TC1 RF board mounted on VD4 mother board

7.2.1.1 RF Device Characterization Board

Figure 7.8 depicts the usage of VD4BJ1DB as an RF Characterization vehicle. The board can be connected to external elements used to perform the characterization process (control and data capture interfaces). This interface to these elements will be described in section 7.2.2.

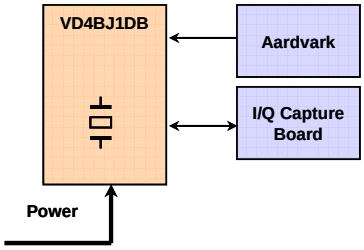

Figure 7.8 – VD4 Bluetooth System

7.2.1.2 Bluetooth System Application Board

Figure 7.2 depicts the complete Bluetooth system that uses VD4BJ1DB as RF link. In this case, VD4BJ1DB is connected to the BlueVD4 motherboard, which is completed with the VD4BTDB (see 7.1) to supply the basic peripherals of a Bluetooth system.

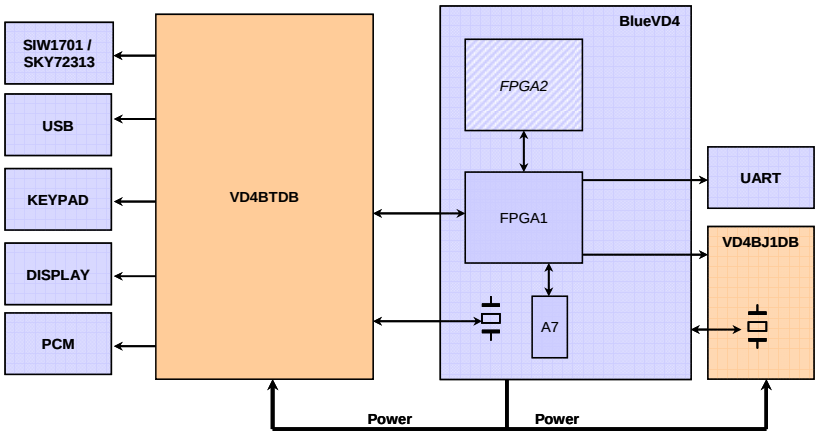

Figure 7.9 – BlueVD4 Bluetooth System

7.2.2 Requirements

7.2.2.1 BB Interface

VD4BJ1DB shall present an interface to the baseband section of the system as described in Table 7.6 below:

Signal Group	Pins	Description
SPI I/F	4	SCLK, MISO, MOSI, N_SS
Data I/F	4	DATAIO[2:0], DATAIO_VAL
Power	2	VDD3V3, GND
Other Control	3	N_RST, ENABLE_RM, GAIN_SET_STS
System Clock	1	BB_CLK

Table 7.6 – Bluejay TC1 Baseband Interface

The baseband interface shall be routed to a 80-pin MOLC_120_02_S_Q_LC male connector (see routing details in section 7.2.3.1), which will be plugged into connector J20 of the VD4 motherboard. All the signals shall be routed to Bluejay TC1 in at least one operating mode, as described in section 7.2.2.2.
In order to ease logic analyzer captures of the baseband interface, all the signals in Table 7.6 will be routed to a 16 pin debug connector.

7.2.2.2 Multiple BB Control Sources

7.2.2.2.1 Multiple BB Control Sources

A provision for an alternative routing to the BlueVD4 interface shall be provided for the following signals:

- ENABLE_RM
- N_RST
- SET_GAIN_STS

A control switch shall be provided in order to route both options accordingly.

7.2.2.2.2 Multiple SPI Sources

The SPI interface of Bluejay TC1 shall be driven by either of the interfaces below. A control switch shall be provided in order to route both options accordingly:

- The baseband interface (see section 7.2.2.1)
- The Aardvark bus (see Figure 7.10,and reference [3])

TOTAL PHASE — Aardvark I²C/SPI Embedded Systems Interface

2 Hardware Specifications

2.1 Pinouts

Connector Specification

The ribbon cable connector is a standard 0.100" (2.54mm) pitch IDC type connector. This connector will mate with a standard keyed boxed header.

Alternatively, a split cable is available which connects to the ribbon cable and provides individual leads for each pin.

Orientation

The ribbon cable pin order follows the standard convention. The red line indicates the first position. When looking at your Aardvark adapter in the upright position (figure 5), pin 1 is in the top left corner and pin 10 is in the bottom right corner.

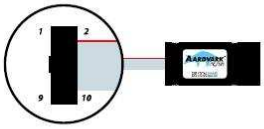

Figure 5: *The Aardvark I2C/SPI Host Adapter in the upright position.*
Pin 1 is located in the upper left corner of the connector and Pin 10 is located in the lower right corner of the connector.

If you flip your Aardvark adapter over (figure 6) such that the text on the serial number label is in the proper upright position, the pin order is as shown in the following diagram.

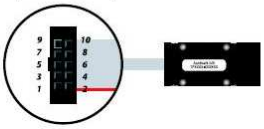

Figure 6: *The Aardvark I2C/SPI Host Adapter in the upside down position.*
Pin 1 is located in the lower left corner of the connector and Pin 10 is located in the upper right corner of the connector.

Order of Leads

1. SCL
2. GND
3. SDA
4. NC/+5V
5. MISO
6. NC/+5V
7. SCLK
8. MOSI
9. SS
10. GND

Figure 7.10 – Aardvark Connector Description

7.2.2.3 Powering Sources

The powering of VD4BJ1DB takes place in two different modes.

7.2.2.3.1 Characterization

The following supply lines of Bluejay TC1 shall be made available independently, to provide power consumption test points:

TC1 Pin	Symbol	Function
2	AVDD_IN_PA	TX driver voltage supply - input
4	AVDD_RXTX	RX/TX block voltage supply – decoupling output
12	VDD_3V3	3.3 V supply (for RF_SW)
28	VDD_IN_DIG	Digital block voltage supply - input
29	VDD_DIG	Digital block voltage supply – decoupling output
31	AVDD_IN_REG	Analog block voltage supply 2 - input
32	AVDD_ADDA	RX ADC/TX DAC voltage supply – decoupling output
34	AVDD_XO	XO block voltage supply – decoupling output
37	AVDD_XX	(Optional pin ## TBD)
38	AVDD_PLL	PLL block voltage supply – decoupling output
39	AVDD_VCO	VCO block voltage supply – decoupling output
40	VREF_RFPLL	RFPLL reference decoupling

Table 7.7 – Bluejay TC1 Power Lines

Group the power per voltage levels

Then, decide how to obtain 1.5, 1.2 from 3v3 (and/or 2v5, and/or 1v8, also available in BlueVD4)

Then decide what method will be used to change.

- from single source
- to multiple source (grouped)
- to multiple source (pin by pin)

7.2.2.3.2 Application Board

All the power lines described in section 7.2.2.3.1 need to be supplied in this mode as a single interface connected to the power section of the baseband connector described in sections 7.2.2.1/7.2.3.1.

7.2.2.4 Spare Area

No spare area for mounting extra components is provided.

7.2.2.5 BlueVD4 Requirements

The requirements specific to BlueVD4 are detailed in Table 7.8 below:

Item	Description
Connection to BlueVD4	VD4BJ1DB can be connected to either J20 (FPGA1) or J22 (FPGA2).

Table 7.8 – BlueVD4 Requirements

7.2.3 Digital signals

The following table lists all the digital signals coming from BlueVD4. It also explains how these signals are mapped on the connector interface between BlueVD4 and VD4BJ1DB.

Digital Interface	Number of signal from BlueVD4	Signal list
Bluejay TC1	15	N_RST, ENABLE_RM, BB_CLK, SCLK, MISO, MOSI, N_SS, DATAIO[3:0], GAIN_SET_STS, NRST_OUT, IO1, IO0
`Spare Control Lines	8	SP_CTRL[7:0]
TOTAL	23	

Table 7.9 – Digital signal list

7.2.3.1 Digital signal corresponding table

The following table explains the relation between VD4BJ1DB and BlueVD4 signals, stating the correspondence between signal names in the schematics, connector pins and FPGA pins. The connector J20 is used to plug VD4BJ1DB on top of the BlueVD4 motherboard. The corresponding bus in the BlueVD4 schematic is FPGA1_1V8_DGHT.

VD4BJ1DB Digital Interface	VD4BJ1DB Signal name	VD4BJ1DB Connector Pin	BlueVD4 connector Pin (I)	FPGA1_1V8_DGHT(i)	FPGA1 Connector Pin
Bluejay TC1	N_RST	J14-C15	J20-C15	46	U17-R/AB8
	N_RST_OUT	J14-A15	J20-A15	14	U17-R/ AE2
	ENABLE_RM	J14-C16	J20-C16	47	U17-R/AC8
	BB_CLK	J14-D12	J20-D12	59	U17-R/AA14
		J14-D13	J20-D13	60	U17-R/AC14
	SCLK	J14-D1	J20-D1	48	U17-R/AE8
	MISO	J14-D3	J20-D3	50	U17-R/AE9
	MOSI	J14-D5	J20-D5	52	U17-R/AC10
	N_SS	J14-D7	J20-D7	54	U17-R/AD11
	DATAIO_3	J14-A1	J20-A1	0	U17-R/W1
	DATAIO_2	J14-A3	J20-A3	2	U17-R/AA1
	DATAIO_1	J14-A5	J20-A5	4	U17-R/AD1
	DATAIO_0	J14-A7	J20-A7	6	U17-R/AF1
	GAIN_SET_STS	J14-C14	J20-C14	45	U17-R/AA8
	IO1	J14-D10	J20-D10	57	U17-R/AB13
	IO0	J14-D9	J20-D9	56	U17-R/AA13
Spare Control Lines	SP_CTRL_7	J14-A13	J20-A13	12	U17-R/AC2
	SP_CTRL_6	J14-B13	J20-B13	28	U17-R/AC4

	SP_CTRL_5	J14-A12	J20-A12	11	U17-R/AB2
	SP_CTRL_4	J14-B12	J20-B12	27	U17-R/AA4
	SP_CTRL_3	J14-A11	J20-A11	10	U17-R/Y2
	SP_CTRL_2	J14-B11	J20-B11	26	U17-R/Y4
	SP_CTRL_1	J14-A10	J20-A10	9	U17-R/W2
	SP_CTRL_0	J14-B10	J20-B10	25	U17-R/W4
TOTAL	23				

Table 7.10 – Digital pin relation between BlueVD4 and VD4BJ1DB

Note that the choice of J20 allows for an eventual split of the entire BT System design by using FPGA2 if necessary (this device is not mounted on BlueVD4 boards). This option can be exercised without any change on VD4BJ1DB, by simple modification of the pin assignments in FPGA1 and FPGA2. VD4BJ1DB will then be connected to FPGA2 through J22 connector.

7.2.3.2 VD4BJ1DB Power correspondence table

Table 7.11shows the power supply signals available in BlueVD4's J20 connector:

VD4BJ1DB Digital Interface	BlueVD4 Signal name	VD4 connector Pin
Power	Vcc_3.3V	J20-D19
	Vcc_2.5V	J20-D20
	Vcc_1.8V_ARMS	J20-B18
	Vio_1.8V	J20-B19
	Vcc_1.2V	J20-B20
Ground	GND	J20-B17
	GND	J20-A17
	GND	J20-A18
	GND	J20-A19
	GND	J20-A20
	GND	J20-D17
	GND	J20-C17
	GND	J20-D18
	GND	J20-C18
	GND	J20-C19
	GND	J20-C20
TOTAL	16	

Table 7.11 – Digital power correspondence between BlueVD4 and VD4BJ1DB

7.2.4 Part list

The following table summarizes the components used in the VD4BJ1DB:

Part Number	RivieraWaves Stock	Description
CON MOLC_120-02-S-Q-LC	TBD	Male connector 80 pin (BlueVD4)
CON FW-30-04-LD-210-160	TBD	Power supply board connectors
CON 8x2-MALE-ALTERNE	TBD	Logic analyzer connector
CON 4x1-MALE	TBD	I/Q board connector
CON 24x2-MALE-ALT-2mm	TBD	HissFPGA board connector
CON 5x2-MALE-ALTERNE	TBD	Aardvark SPI, 0.100” (2.54mm) pitch IDC type connector
LTC3543EDCB	TBD	DC-DC converter
MAX3392E	TBD	Level shifter
NX2520DA	TBD	52MHz quartz
BOOST2RF-QFN40	Y	BlueJay TC1
DEA252450BT_7012D1	TBD	Multilayer band-pass filter 2.4 GHz from TDK
LFL182G45TC1A108	TBD	Low Pass Filter muRata
HHM1711D1	TBD	100:50 TDK 2.4GHz Balun
SST12LP15A	TBD	External PA SST 2.4 GHz

Table 7.12 – VD4BJ1DB Part list

8 Connector connections

8.1 Digital interface

The following table summarizes the digital interface connections, particularly on which pin number of FPGA1 it is connected.

- ✓ Connector type: AMP_104693-8
- ✓ Schematics reference: J5 & J6

The pinout of these two connectors is forecast to be connected to the PCCextend 125A from Sycard to have a PCMCIA interface. For more information of PCCextend 125A, see [1].

GND: connected to board ground
3V3: connected to the 3.3V of the board
NC: not connected
FPGA1: XC4VLX200-11FF1513C
CPLD: XC95288XL-6FG256C

Connector pin number	Signal name	Board connection
J5-1	GND	
J5-2	GND	
J5-3	NC	
J5-4	GND	
J5-5	GND	
J5-6	GND	
J5-7	CAD27_IO21	FPGA1-AV37
J5-8	nCCLKRUN_IO0	FPGA1-AR32
J5-9	GND	
J5-10	GND	
J5-11	CAD25_IO22	FPGA1-AU36
J5-12	CAD29_IO1	FPGA1-AT30
J5-13	GND	
J5-14	GND	
J5-15	CAD23_IO23	FPGA1-AU33
J5-16	CAD26_IO2	FPGA1-AT26
J5-17	GND	
J5-18	GND	
J5-19	CAD21_IO24	FPGA1-AU31
J5-20	CAD24_IO3	FPGA1-AT24
J5-21	GND	
J5-22	GND	
J5-23	CAD18_IO25	FPGA1-AU27
J5-24	CAD22_IO4	FPGA1-AU32
J5-25	GND	
J5-26	GND	
J5-27	nCIRDY_IO26	FPGA1-AP25
J5-28	CAD20_IO5	FPGA1-AU30
J5-29	GND	
J5-30	GND	
J5-31	NC	
J5-32	nCCBE2_IO6	FPGA1-AR27
J5-33	GND	
J5-34	GND	
J5-35	nCINT_IO27	FPGA1-AP24
J5-36	CCLK_IO7	FPGA1-AH20 (Global CLK)
J5-37	GND	
J5-38	GND	
J5-39	NCPERR_IO28	FPGA1-AW24

J5-40	3V3	
J5-41	GND	
J5-42	GND	
J5-43	nCCBE1_IO29	FPGA1-AR26
J5-44	nCGNT_IO8	FPGA1-AR31
J5-45	GND	
J5-46	GND	
J5-47	CAD12_IO30	FPGA1-AV30
J5-48	CPAR_IO9	FPGA1-AR29
J5-49	GND	
J5-50	GND	
J5-51	CAD9_IO31	FPGA1-AV27
J5-52	CAD14_IO10	FPGA1-AV33
J5-53	GND	
J5-54	GND	
J5-55	CAD7_IO32	FPGA1-AW34
J5-56	CAD11_IO11	FPGA1-AV29
J5-57	GND	
J5-58	GND	
J5-59	CAD3_IO33	FPGA1-AW29
J5-60	nCCBE0_IO12	FPGA1-AR24
J5-61	GND	
J5-62	GND	
J5-63	CAD0_IO34	FPGA1-AP36
J5-64	CAD5_IO13	FPGA1-AW31
J5-65	GND	
J5-66	GND	
J5-67	GND	
J5-68	CAD1_IO14	FPGA1-AW26
J5-69	IO35	FPGA1-AU35
J5-70	IO15	FPGA1-AR33
J5-71	IO36	FPGA1-AT25
J5-72	IO16	FPGA1-AP29
J5-73	IO37	FPGA1-AU28
J5-74	IO17	FPGA1-AT31
J5-75	IO38	FPGA1-AR28
J5-76	IO18	FPGA1-AV28
J5-77	IO39	FPGA1-AT34
J5-78	IO19	FPGA1-AV35
J5-79	IO40	FPGA1-AT35
J5-80	IO20	FPGA1-AT28
J6-1	GND	
J6-2	GND	
J6-3	GND	
J6-4	nCCD2	CPLD-N16
J6-5	GND	
J6-6	GND	
J6-7	CAD31_IO58	FPGA1-AT33
J6-8	CAD30_IO41	FPGA1-AW36
J6-9	GND	
J6-10	GND	
J6-11	CAD28_IO59	FPGA1-AT38
J6-12	CSTSCHG_IO42	FPGA1-AP31
J6-13	GND	
J6-14	GND	
J6-15	CAUDIO_IO60	FPGA1-AN30
J6-16	nCCBE3_IO43	FPGA1-AU38

J6-17	GND	
J6-18	GND	
J6-19	nCREQ_IO61	FPGA1-AR39
J6-20	nCSERR_IO44	FPGA1-AW35
J6-21	GND	
J6-22	GND	
J6-23	nCRST	CPLD-J16
J6-24	CVS2	CPLD-L16
J6-25	GND	
J6-26	GND	
J6-27	CAD19_IO62	FPGA1-AU37
J6-28	CAD17_IO45	FPGA1-AU26
J6-29	GND	
J6-30	GND	
J6-31	nFRAME_IO63	FPGA1-AT39
J6-32	nCTRDY_IO46	FPGA1-AP27
J6-33	GND	
J6-34	GND	
J6-35	NC	
J6-36	3V3	
J6-37	GND	
J6-38	GND	
J6-39	nCDEVSEL_IO64	FPGA1-AR38
J6-40	nCSTOP_IO47	FPGA1-AP26
J6-41	GND	
J6-42	GND	
J6-43	nCBLOCK_IO65	FPGA1-AP32
J6-44	NC	
J6-45	GND	
J6-46	GND	
J6-47	CAD16_IO66	FPGA1-AR37
J6-48	CAD15_IO48	FPGA1-AV34
J6-49	GND	
J6-50	GND	
J6-51	CAD13_IO67	FPGA1-AV32
J6-52	CVS1	CPLD-K16
J6-53	GND	
J6-54	GND	
J6-55	CAD10_IO68	FPGA1-AW37
J6-56	CAD8_IO49	FPGA1-AV25
J6-57	GND	
J6-58	GND	
J6-59	NC	
J6-60	CAD6_IO50	FPGA1-AW32
J6-61	GND	
J6-62	GND	
J6-63	CAD4_IO69	FPGA1-AP37
J6-64	CAD2_IO51	FPGA1-AW27
J6-65	GND	
J6-66	GND	
J6-67	nCCD1	CPLD-M16
J6-68	GND	
J6-69	IO70	FPGA1-AN27
J6-70	IO52	FPGA1-AT36
J6-71	IO71	FPGA1-AN29
J6-72	IO53	FPGA1-AT29
J6-73	IO72	FPGA1-AP34

J6-74	IO54	FPGA1-AN28
J6-75	IO73	FPGA1-AP35
J6-76	IO55	FPGA1-AR34
J6-77	IO74	FPGA1-AW25
J6-78	IO56	FPGA1-AR36
J6-79	IO75	FPGA1-AW30
J6-80	IO57	FPGA1-AU25

Table 8.1 – Digital Port connections

8.2 Test Connectors

The following tables summarize the test connector connections, particularly on which pin number of FPGA1 and FPGA2 it is connected.

8.2.1 FPGA1

Connector type: AMP 767054-1 (Mictor Connector)

Schematic references: J8 & J9 & J10

GND: connected to board ground
FPGA1: XC4VLX200-11FF1513C

Connector pin number	Signal name	FPGA1 connection	Mictor connection
J8-1	GND		
J8-2	GND		
J8-3	FPGA1_TEST0	FPGA1-U10	A:CLK0
J8-4	FPGA1_TEST1	FPGA1-U8	A3:7
J8-5	FPGA1_TEST2	FPGA1-U7	A3:6
J8-6	FPGA1_TEST3	FPGA1-U6	A3:5
J8-7	FPGA1_TEST4	FPGA1-U5	A3:4
J8-8	FPGA1_TEST5	FPGA1-U3	A3:3
J8-9	FPGA1_TEST6	FPGA1-U2	A3:2
J8-10	FPGA1_TEST7	FPGA1-U1	A3:1
J8-11	FPGA1_TEST8	FPGA1-V13	A3:0
J8-12	FPGA1_TEST9	FPGA1-V12	A2:7
J8-13	FPGA1_TEST10	FPGA1-V10	A2:6
J8-14	FPGA1_TEST11	FPGA1-V9	A2:5
J8-15	FPGA1_TEST12	FPGA1-V7	A2:4
J8-16	FPGA1_TEST13	FPGA1-V5	A2:3
J8-17	FPGA1_TEST14	FPGA1-W12	A2:2
J8-18	FPGA1_TEST15	FPGA1-W10	A2:1
J8-19	FPGA1_TEST16	FPGA1-W9	A2:0
J8-20	FPGA1_TEST17	FPGA1-W7	A0:0
J8-21	FPGA1_TEST18	FPGA1-W6	A0:1
J8-22	FPGA1_TEST19	FPGA1-W5	A0:2
J8-23	FPGA1_TEST20	FPGA1-Y13	A0:3
J8-24	FPGA1_TEST21	FPGA1-Y11	A0:4
J8-25	FPGA1_TEST22	FPGA1-Y9	A0:5
J8-26	FPGA1_TEST23	FPGA1-AA11	A0:6
J8-27	FPGA1_TEST24	FPGA1-AA10	A0:7
J8-28	FPGA1_TEST25	FPGA1-AD17	A1:0
J8-29	FPGA1_TEST26	FPGA1-AE18	A1:1

J8-30	FPGA1_TEST27	FPGA1-AE12	A1:2
J8-31	FPGA1_TEST28	FPGA1-AE11	A1:3
J8-32	FPGA1_TEST29	FPGA1-AF11	A1:4
J8-33	FPGA1_TEST30	FPGA1-AF9	A1:5
J8-34	FPGA1_TEST31	FPGA1-AF8	A1:6
J8-35	FPGA1_TEST32	FPGA1-AG17	A1:7
J8-36	FPGA1_TEST33	FPGA1-AF23	A:CLK1
J8-37	GND		
J8-38	GND		
J9-1	GND		
J9-2	GND		
J9-3	FPGA1_TEST34	FPGA1-AG10	C:CLK3
J9-4	FPGA1_TEST35	FPGA1-AG8	C3:7
J9-5	FPGA1_TEST36	FPGA1-AG7	C3:6
J9-6	FPGA1_TEST37	FPGA1-AG6	C3:5
J9-7	FPGA1_TEST38	FPGA1-AG5	C3:4
J9-8	FPGA1_TEST39	FPGA1-AH17	C3:3
J9-9	FPGA1_TEST40	FPGA1-AJ22	C3:2
J9-10	FPGA1_TEST41	FPGA1-AH13	C3:1
J9-11	FPGA1_TEST42	FPGA1-AH10	C3:0
J9-12	FPGA1_TEST43	FPGA1-AH9	C2:7
J9-13	FPGA1_TEST44	FPGA1-AH7	C2:6
J9-14	FPGA1_TEST45	FPGA1-AH5	C2:5
J9-15	FPGA1_TEST46	FPGA1-AH4	C2:4
J9-16	FPGA1_TEST47	FPGA1-AH3	C2:3
J9-17	FPGA1_TEST48	FPGA1-AH2	C2:2
J9-18	FPGA1_TEST49	FPGA1-AJ16	C2:1
J9-19	FPGA1_TEST50	FPGA1-AJ12	C2:0
J9-20	FPGA1_TEST51	FPGA1-AJ10	C0:0
J9-21	FPGA1_TEST52	FPGA1-AJ9	C0:1
J9-22	FPGA1_TEST53	FPGA1-AJ7	C0:2
J9-23	FPGA1_TEST54	FPGA1-AJ6	C0:3
J9-24	FPGA1_TEST55	FPGA1-AJ5	C0:4
J9-25	FPGA1_TEST56	FPGA1-AJ4	C0:5
J9-26	FPGA1_TEST57	FPGA1-AJ2	C0:6
J9-27	FPGA1_TEST58	FPGA1-AJ1	C0:7
J9-28	FPGA1_TEST59	FPGA1-AK17	C1:0
J9-29	FPGA1_TEST60	FPGA1-AK16	C1:1
J9-30	FPGA1_TEST61	FPGA1-AK11	C1:2
J9-31	FPGA1_TEST62	FPGA1-AK9	C1:3
J9-32	FPGA1_TEST63	FPGA1-AK8	C1:4
J9-33	FPGA1_TEST64	FPGA1-AK7	C1:5
J9-34	FPGA1_TEST65	FPGA1-AK6	C1:6
J9-35	FPGA1_TEST66	FPGA1-AK4	C1:7
J9-36	FPGA1_TEST67	FPGA1-AK3	C:Q1
J9-37	GND		
J9-38	GND		
J10-1	GND		
J10-2	GND		
J10-3	FPGA1_TEST68	FPGA1-AK2	D:Q0
J10-4	FPGA1_TEST69	FPGA1-AK1	D3:7
J10-5	FPGA1_TEST70	FPGA1-AL18	D3:6
J10-6	FPGA1_TEST71	FPGA1-AL16	D3:5
J10-7	FPGA1_TEST72	FPGA1-AL14	D3:4
J10-8	FPGA1_TEST73	FPGA1-AL13	D3:3
J10-9	FPGA1_TEST74	FPGA1-AL11	D3:2
J10-10	FPGA1_TEST75	FPGA1-AL10	D3:1

J10-11	FPGA1_TEST76	FPGA1-AL9	D3:0
J10-12	FPGA1_TEST77	FPGA1-AL8	D2:7
J10-13	FPGA1_TEST78	FPGA1-AL6	D2:6
J10-14	FPGA1_TEST79	FPGA1-AL5	D2:5
J10-15	FPGA1_TEST80	FPGA1-AL4	D2:4
J10-16	FPGA1_TEST81	FPGA1-AL3	D2:3
J10-17	FPGA1_TEST82	FPGA1-AL1	D2:2
J10-18	FPGA1_TEST83	FPGA1-AM21	D2:1
J10-19	FPGA1_TEST84	FPGA1-AM20	D2:0
J10-20	FPGA1_TEST85	FPGA1-AM18	D0:0
J10-21	FPGA1_TEST86	FPGA1-AM17	D0:1
J10-22	FPGA1_TEST87	FPGA1-AM15	D0:2
J10-23	FPGA1_TEST88	FPGA1-AM13	D0:3
J10-24	FPGA1_TEST89	FPGA1-AM11	D0:4
J10-25	FPGA1_TEST90	FPGA1-AM10	D0:5
J10-26	FPGA1_TEST91	FPGA1-AM7	D0:6
J10-27	FPGA1_TEST92	FPGA1-AM6	D0:7
J10-28	FPGA1_TEST93	FPGA1-AM5	D1:0
J10-29	FPGA1_TEST94	FPGA1-AM3	D1:1
J10-30	FPGA1_TEST95	FPGA1-AM2	D1:2
J10-31	FPGA1_TEST96	FPGA1-AM1	D1:3
J10-32	FPGA1_TEST97	FPGA1-AN7	D1:4
J10-33	FPGA1_TEST98	FPGA1-AN5	D1:5
J10-34	FPGA1_TEST99	FPGA1-AN4	D1:6
J10-35	FPGA1_TEST100	FPGA1-AN3	D1:7
J10-36	FPGA1_TEST101	FPGA1-AN2	D:CLK2
J10-37	GND		
J10-38	GND		

Table 8.2 – FPGA1 test connectors

8.2.2 FPGA2

Connector type: AMP 767054-1 (Mictor Connector)

Schematic references: J12 & J13 & J14

GND: connected to board ground
FPGA2: XC4VLX200-11FF1513C

Connector pin number	Signal name	FPGA2 connection	Mictor connection
J12-1	GND		
J12-2	GND		
J12-3	FPGA2_TEST0	FPGA2-R6	A:CLK0
J12-4	FPGA2_TEST1	FPGA2-R4	A3:7
J12-5	FPGA2_TEST2	FPGA2-R3	A3:6
J12-6	FPGA2_TEST3	FPGA2-R2	A3:5
J12-7	FPGA2_TEST4	FPGA2-R1	A3:4
J12-8	FPGA2_TEST5	FPGA2-T9	A3:3
J12-9	FPGA2_TEST6	FPGA2-T8	A3:2
J12-10	FPGA2_TEST7	FPGA2-T6	A3:1
J12-11	FPGA2_TEST8	FPGA2-T5	A3:0
J12-12	FPGA2_TEST9	FPGA2-T4	A2:7
J12-13	FPGA2_TEST10	FPGA2-T3	A2:6
J12-14	FPGA2_TEST11	FPGA2-T1	A2:5
J12-15	FPGA2_TEST12	FPGA2-U10	A2:4

J12-16	FPGA2_TEST13	FPGA2-U8	A2:3
J12-17	FPGA2_TEST14	FPGA2-U7	A2:2
J12-18	FPGA2_TEST15	FPGA2-U6	A2:1
J12-19	FPGA2_TEST16	FPGA2-U5	A2:0
J12-20	FPGA2_TEST17	FPGA2-U3	A0:0
J12-21	FPGA2_TEST18	FPGA2-U2	A0:1
J12-22	FPGA2_TEST19	FPGA2-U1	A0:2
J12-23	FPGA2_TEST20	FPGA2-V13	A0:3
J12-24	FPGA2_TEST21	FPGA2-V12	A0:4
J12-25	FPGA2_TEST22	FPGA2-V10	A0:5
J12-26	FPGA2_TEST23	FPGA2-V9	A0:6
J12-27	FPGA2_TEST24	FPGA2-V7	A0:7
J12-28	FPGA2_TEST25	FPGA2-V5	A1:0
J12-29	FPGA2_TEST26	FPGA2-V4	A1:1
J12-30	FPGA2_TEST27	FPGA2-V3	A1:2
J12-31	FPGA2_TEST28	FPGA2-V2	A1:3
J12-32	FPGA2_TEST29	FPGA2-W12	A1:4
J12-33	FPGA2_TEST30	FPGA2-W10	A1:5
J12-34	FPGA2_TEST31	FPGA2-W9	A1:6
J12-35	FPGA2_TEST32	FPGA2-W7	A1:7
J12-36	FPGA2_TEST33	FPGA2-W6	A:CLK1
J12-37	GND		
J12-38	GND		
J13-1	GND		
J13-2	GND		
J13-3	FPGA2_TEST34	FPGA2-W5	C:CLK3
J13-4	FPGA2_TEST35	FPGA2-W4	C3:7
J13-5	FPGA2_TEST36	FPGA2-W2	C3:6
J13-6	FPGA2_TEST37	FPGA2-W1	C3:5
J13-7	FPGA2_TEST38	FPGA2-Y13	C3:4
J13-8	FPGA2_TEST39	FPGA2-Y11	C3:3
J13-9	FPGA2_TEST40	FPGA2-Y9	C3:2
J13-10	FPGA2_TEST41	FPGA2-Y7	C3:1
J13-11	FPGA2_TEST42	FPGA2-Y6	C3:0
J13-12	FPGA2_TEST43	FPGA2-Y4	C2:7
J13-13	FPGA2_TEST44	FPGA2-Y3	C2:6
J13-14	FPGA2_TEST45	FPGA2-Y2	C2:5
J13-15	FPGA2_TEST46	FPGA2-Y1	C2:4
J13-16	FPGA2_TEST47	FPGA2-AA14	C2:3
J13-17	FPGA2_TEST48	FPGA2-AA13	C2:2
J13-18	FPGA2_TEST49	FPGA2-AA11	C2:1
J13-19	FPGA2_TEST50	FPGA2-AA10	C2:0
J13-20	FPGA2_TEST51	FPGA2-AA8	C0:0
J13-21	FPGA2_TEST52	FPGA2-AA6	C0:1
J13-22	FPGA2_TEST53	FPGA2-AA5	C0:2
J13-23	FPGA2_TEST54	FPGA2-AA4	C0:3
J13-24	FPGA2_TEST55	FPGA2-AA3	C0:4
J13-25	FPGA2_TEST56	FPGA2-AA1	C0:5
J13-26	FPGA2_TEST57	FPGA2-AB15	C0:6
J13-27	FPGA2_TEST58	FPGA2-AB13	C0:7
J13-28	FPGA2_TEST59	FPGA2-AB11	C1:0
J13-29	FPGA2_TEST60	FPGA2-AB10	C1:1
J13-30	FPGA2_TEST61	FPGA2-AB8	C1:2
J13-31	FPGA2_TEST62	FPGA2-AB7	C1:3
J13-32	FPGA2_TEST63	FPGA2-AB6	C1:4
J13-33	FPGA2_TEST64	FPGA2-AB5	C1:5
J13-34	FPGA2_TEST65	FPGA2-AB3	C1:6

J13-35	FPGA2_TEST66	FPGA2-AB2	C1:7
J13-36	FPGA2_TEST67	FPGA2-AB1	C:Q1
J13-37	GND		
J13-38	GND		
J14-1	GND		
J14-2	GND		
J14-3	FPGA2_TEST68	FPGA2-AC14	D:Q0
J14-4	FPGA2_TEST69	FPGA2-AC13	D3:7
J14-5	FPGA2_TEST70	FPGA2-AC12	D3:6
J14-6	FPGA2_TEST71	FPGA2-AC10	D3:5
J14-7	FPGA2_TEST72	FPGA2-AC8	D3:4
J14-8	FPGA2_TEST73	FPGA2-AC7	D3:3
J14-9	FPGA2_TEST74	FPGA2-AC5	D3:2
J14-10	FPGA2_TEST75	FPGA2-AC4	D3:1
J14-11	FPGA2_TEST76	FPGA2-AC3	D3:0
J14-12	FPGA2_TEST77	FPGA2-AC2	D2:7
J14-13	FPGA2_TEST78	FPGA2-AD11	D2:6
J14-14	FPGA2_TEST79	FPGA2-AD9	D2:5
J14-15	FPGA2_TEST80	FPGA2-AD7	D2:4
J14-16	FPGA2_TEST81	FPGA2-AD6	D2:3
J14-17	FPGA2_TEST82	FPGA2-AD5	D2:2
J14-18	FPGA2_TEST83	FPGA2-AD4	D2:1
J14-19	FPGA2_TEST84	FPGA2-AD2	D2:0
J14-20	FPGA2_TEST85	FPGA2-AD1	D0:0
J14-21	FPGA2_TEST86	FPGA2-AE12	D0:1
J14-22	FPGA2_TEST87	FPGA2-AE11	D0:2
J14-23	FPGA2_TEST88	FPGA2-AE9	D0:3
J14-24	FPGA2_TEST89	FPGA2-AE8	D0:4
J14-25	FPGA2_TEST90	FPGA2-AE6	D0:5
J14-26	FPGA2_TEST91	FPGA2-AE4	D0:6
J14-27	FPGA2_TEST92	FPGA2-AE3	D0:7
J14-28	FPGA2_TEST93	FPGA2-AE2	D1:0
J14-29	FPGA2_TEST94	FPGA2-AE1	D1:1
J14-30	FPGA2_TEST95	FPGA2-AF11	D1:2
J14-31	FPGA2_TEST96	FPGA2-AF9	D1:3
J14-32	FPGA2_TEST97	FPGA2-AF8	D1:4
J14-33	FPGA2_TEST98	FPGA2-AF6	D1:5
J14-34	FPGA2_TEST99	FPGA2-AF5	D1:6
J14-35	FPGA2_TEST100	FPGA2-AF4	D1:7
J14-36	FPGA2_TEST101	FPGA2-AF3	D:CLK2
J14-37	GND		
J14-38	GND		

Table 8.3 – FPGA2 test connectors

9 Problems on board

9.1 Nothing is running

Verify you are using the appropriate power supply:

- ✓ Transformer part reference: SB-035A0F-11, 3V3 @ 5A from Stontronics
- ✓ Jack connector + inside, - outside

Check the following green power LEDs on the upper right corner are ON:

- ✓ 3V3
- ✓ 2V5
- ✓ 1V8 IO
- ✓ 1V8 ARM
- ✓ 1V2

9.2 FPGA problem

Orange LED DONE or FPGA Configuration (near CPLD) is not ON after power up:

- ✓ Check that all the “power LEDs” are ON.
- ✓ Check that the following filters are presents (back side of the board): F1, F2, F3, F4, F7 and F8.
- ✓ Reload the FPGA binary inside HW-FLASH with the BLUE POD, and check that there are no errors during loading, see Programming HW Flash chapter.
- ✓ Reload the CPLD via CPLD JTAG chain with appropriate program, see CPLD JTAG Chain chapter.
- ✓ Check the programming oscillator clock is correctly running: 8Mhz on test point CCLK near CPLD.

References

[1]	**Title**	PCC Extend 125HIB User's manual		
	Reference	M200049-03		
	Version	1	**Date**	December 2001
	Source	Sycard, www.sycard.com		

[2]	**Title**	FT245BM USB FIFO (USB - Parallel) I.C.		
	Reference	DS245B		
	Version	1.6	**Date**	2005
	Source	Future Technology Devices Intl. Ltd.		

[3]	**Title**	Aardvark I2C/SPI Embedded Systems Interface		
	Reference			
	Version	V3.20	**Date**	July 15, 2005
	Source	Total Phase		